REMARKS

The Official Action dated April 2, 2007 has been received and its contents carefully noted. In view thereof, claim 1 has been amended in order to better define that which Applicants regard as the invention. As previously, claims 1-11 are presently pending in the instant application.

Turning now to the Official Action and particularly page 2 thereof, claims 1, 2, and 4-8 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,726,942 issued to Yoneda et al. This rejection is respectfully traversed in that the patent to Yoneda et al. neither discloses nor remotely suggests that which is presently set forth by Applicants' claimed invention.

As can be seen from the foregoing amendments, independent claim 1 has been amended to recite an arbiter circuit comprising data transfer request signal holding means for accepting a plurality of data transfer request signals and holding the data transfer request signals in response to predetermined timing signals, a prioritizing means for determining only a signal with the highest priority at a certain point as a valid signal and the signals with lower priorities as invalid signals in order to assign priorities to output signals from the data transfer request signal holding means, controlling means for outputting a controlling signal to the data transfer request signal holding means based on the signals output from the prioritizing means and delaying means for generating a data transfer execution signals from the output signals of the prioritizing means. That is, in the arbiter circuit set forth in accordance with Applicants' claimed invention, the data transfer request signal holding means is controlled by the controlling signal generated by the controlling means. The controlling means is assigned to the gate circuit, that is, in accordance with the disclosed embodiment, the gate circuit 23a and 23b. When one of the signals ARB_NO < 1 > is activated, signal TRE and TREb are switched "L" level and a "H" level, respectively. Subsequently, at the transfer gates TR < 0 >

- TR < 2 > blocks the inputs of the data transfer request signals ARBI < 0 > - ARBI < 2 >, and the holding circuits CINV0-CINV2 respectively latch the current status.

In reviewing the teachings of Yoneda et al. and particularly the encoder set forth therein, it is respectfully submitted that such a device fails to include or suggest a controlling means for outputting a controlling signal to the data transfer request signal holding means based on the signals output from the prioritizing means as is specifically recited by Applicants' claimed invention. Accordingly, it is respectfully submitted that independent claim 1 as well as those claims which depend therefrom clearly distinguishes over the teachings of Yoneda et al. and that such disclosure fails to include all the limitations presently set forth in independent claim 1. Therefore, it is respectfully submitted that independent claim 1 as well as those claims which depend therefrom are in proper condition for allowance.

With reference to page 6 of the Office Action, claims 3 and 9-11 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Yoneda et al. in view of Japanese Patent Publication 1993-259900 to Okabayashi et al. This rejection is respectfully traversed in that the publication to Okabayashi et al. fails to overcome the aforementioned shortcomings associated with the teachings of Yoneda et al.

That is, while Okabayashi et al. may disclose a circuit comprising an even number of conduction resistors controlled CMOS inverters connected in a series, this reference fails to disclose or suggest that which is presently set forth by Applicants' claimed invention. Specifically, even if the teachings of Yoneda et al. are modified in the manner suggested by the Examiner in view of the teachings of Okabayashi et al., such combination fails to include or suggest an arbiter circuit including a data transfer request signal holding means, a prioritizing means for determining only a signal with the highest priority at a certain point as a valid signal and the signals with lower priorities as invalid signals in order to assign

priorities to output signals from the data transfer request signal holding means, a controlling means for outputting a controlling signal to the data transfer request signal holding means based on the signals output from the prioritizing means and a delaying means for generating data transfer execution signals from the output signals of the prioritizing means as currently recited by Applicants' claimed invention. Accordingly, it is respectfully submitted that Applicants' claimed invention as set forth in independent claim 1 as well as claims 3 and 9-11 which depend therefrom, clearly distinguishes over the combination proposed by the Examiner and is in proper condition for allowance.

Therefore, in view of the foregoing it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-11 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,

Donald R. Studebaker
Reg. No. 32,815

Nixon Peabody LLP
401 9th Street N.W.
Suite 900
Washington, D. C. 20004
(202) 585-8000